MOTOROLA

# Professional Radio
# GP Series

## Lowband (29.7-42MHz and 35-50MHz)
## Service Information

Issue: June 2002

# Computer Software Copyrights

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# Chapter 1

# MODEL CHART AND TECHNICAL SPECIFICATIONS

## 1.0 GP340 / GP380 Model Chart

| Professional GP300 Series (LB) | | | | | | |
|---|---|---|---|---|---|---|
| **Model** | | | | | | **Description** |
| MDH25BEC9AN3_E | | | | | | GP340 LB1 29.7-42 MHz 6W 16-Ch |
| | MDH25BEH9AN6_E | | | | | GP380 LB1 29.7-42 MHz 6W 255-Ch |
| | | MDH25CEC9AN3_E | | | | GP340 LB2 35-50 MHz 6W 16-Ch |
| | | | MDH25CEH9AN6_E | | | GP380 LB2 35-50 MHz 6W 255-Ch |
| | | | | | | |
| | | | | | **Item** | **Description** |
| X | | | | | PMLB4006_ | GP340 LB1 Back Cover Kit |
| | X | | | | PMLB4016_ | GP380 LB1 Back Cover Kit |
| | | X | | | PMLB4012_ | GP340 LB2 Back Cover Kit |
| | | | X | | PMLB4017_ | GP380 LB2 Back Cover Kit |
| X | | X | | | 6864110B13 | GP340 Basic User Guide |
| | X | | X | | 6864110B18 | GP380 Basic User Guide |
| X | X | X | X | | NAB6064_ | Low/Mid Band (29-50MHz) Heliflex, Trimmable Antenna |
| X | X | X | X | | HNN9008_ | Battery, NiMH Standard |

x = Indicates one of each is required.

## 2.0 Technical Specifications

Data is specified for +25°C unless otherwise stated.

| General Specifications | | |
|---|---|---|
| Channel Capacity<br>**GP340**<br>**GP380** | <br>16<br>255 | |
| Power Supply | Rechargeable battery 7.5v | |
| Dimensions: H x W x D (mm)<br>With standard high capacity NiMH battery<br>With ultra high capacity NiMH battery<br>With NiCD battery<br>With LiIon battery | Height excluding knobs<br>137 x 57.5 x 37.5<br>137 x 57.5 x 40.0<br>137 x 57.5 x 40.0<br>137 x 57.5 x 33.0 | |
| Weight: (gm)<br>With Standard high capacity NiMH battery<br>With Ultra high capacity NiMH battery<br>With NiCD battery<br>With LiIon battery | **GP340**<br>420<br>500<br>450<br>350 | **GP380**<br>428<br>508<br>458<br>358 |
| Average Battery Life @5/5/90 Cycle:<br>With Standard high capacity NiMH battery<br>With Ultra high capacity NiMH battery<br>With NiCD battery<br>With LiIon battery | Low Power<br>11 hours<br>14 hours<br>12 hours<br>11 hours | High Power<br>8 hours<br>11 hours<br>9 hours<br>8 hours |
| Sealing: | Withstands rain testing per<br>MIL STD 810 C/D /E and IP54 | |
| Shock and Vibration: | Protection provided via impact resistant housing exceeding MIL STD 810-C/D /E and TIA/EIA 603 | |
| Dust and Humidity: | Protection provided via environment resistant housing exceeding MIL STD 810 C/D /E and TIA/EIA 603 | |
| | | |
| | | |

| Transmitter | LB |
|---|---|
| *Frequencies - Full Bandsplit | LB1 29.7-42 MHz<br>LB2 35-50 MHz |
| Channel Spacing | 12.5/20/25 kHz |
| Frequency Stability<br>(-25°C to +55°C, +25° Ref.) | ±10ppm |
| Power | 1-6W |
| Modulation Limiting | ±2.5 @ 12.5 kHz<br>±4.0 @ 20 kHz<br>±5.0 @ 25 kHz |
| FM Hum & Noise | -40 dB typical |
| Conducted/Radiated Emission | -36 dBm <1 GHz<br>-30 dBm >1 GHz |
| Adjacent Channel Power | -60 dB @ 12.5 kHz<br>-70 dB @ 25 kHz |
| Audio Response (300 - 3000 Hz) | +1 to -3 dB |
| Audio Distortion | <3% typical |

| Receiver | LB |
|---|---|
| *Frequencies - Full Bandsplit | LB1 29.7-42 MHz<br>LB2 35-50 MHz |
| Channel Spacing | 12.5/20/25 kHz |
| Sensitivity (12 dB SINAD) EIA<br>Sensitivity (20 dB SINAD) ETS | 0.25 µV typical<br>0.50 µV typical |
| Intermodulation EIA | 65 dB |
| Adjacent Channel Selectivity | 60 dB @ 12.5 kHz<br>70 dB @ 25 kHz |
| Spurious Rejection | >70 dB |
| Rated Audio | 0.5W |
| Audio Distortion @ Rated Audio | <3% typical |
| Hum & Noise | -45 dB @ 12.5 kHz<br>-50 dB @ 20/25 kHz |
| Audio Response (300 - 3000 Hz) | +1 to -3 dB |
| Conducted Spurious Emission | -57 dBm <1 GHz<br>-47 dBm >1 GHz<br>ETS 300 086 |

*Availability subject to the laws and regulations of individual countries.

# Chapter 2
# THEORY OF OPERATION

## 1.0 Introduction

This chapter provides a detailed theory of operation for the radio RF circuits. Refer to the relevant section of this manual for details of the operation of the Controller Circuits.

## 2.0 Lowband Transmitter

(*Refer to Figure 2-1 and the Lowband Transmitter schematic diagram*)

The Lowband transmitter consists of the following basic circuits :

- Power amplifier (PA).
- Antenna switch/harmonic filter.
- Antenna matching network.
- Power Control Integrated Circuit (PCIC).

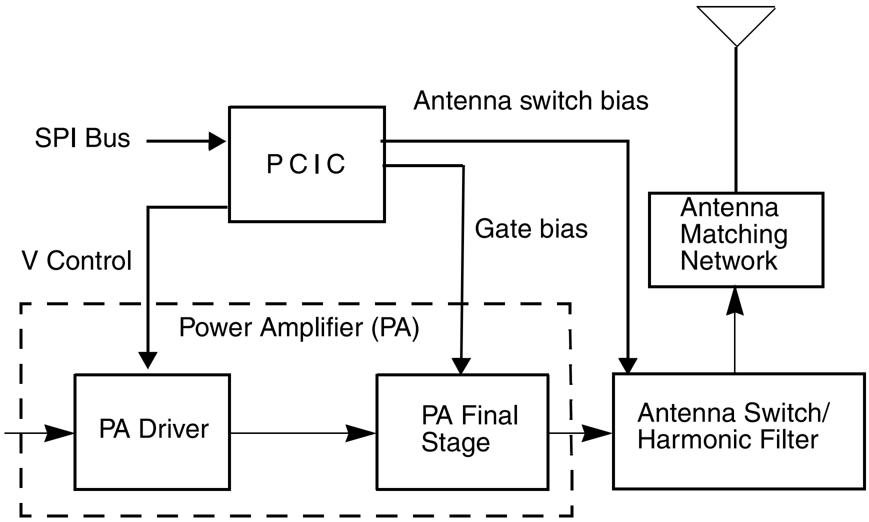



**Figure 2-1** Lowband Transmitter Block Diagram.

### 2.1 Power Amplifier (PA)

The power amplifier (PA) consists of two LDMOS devices:

1. PA driver IC, U101.
2. PA final stage, Q100.

The LDMOS driver (U101) provides 2-stage amplification using a supply voltage of 7.3V. The amplifier is capable of supplying an output power of 0.3W (pins 6 and 7) with an input signal of 2mW at (pin16). The current drain is typically 120mA while operating in the frequency range of 29.7 - 50 MHz. The power output of this stage is varied by the power control loop which controls the voltage on pin 1.

The LDMOS PA is capable of supplying an output power of 8W with an input signal of 0.3W. The current drain is typically 2000 mA while operating in the frequency range of 29.7 - 50 MHz. The final stage gate is bias by a voltage from PCIC pin 24. This voltage is the output of a programmable DAC inside the PCIC and the output is adjustable with the radio tuner.

## 2.2 Antenna Switch

The antenna switch circuit consists of two pin diodes (D100 and D101), a RF network (C147 and L103), and a DC feed network (L104, C144 and current limiting resistor R101). In the transmit mode, PCIC (U102) pin 32 goes high supplying current via the feed network to bias the diodes “on”. The shunt diode (D101) shorts out the receiver port and L103 is connected from the RF path to ground. L103 and the input capacitance of the lowpass filter form a parallel resonant circuit, effectively disconnecting the receiver port from the antenna while not loading the transmit path. In the receive mode, pin 32 goes low and the diodes are off. D100 looks like a high impedance disconnecting the transmitter from the antenna while L103 and C147 form a series resonant circuit to connect the receiver to the antenna.

## 2.3 Harmonic Filter

The harmonic filter consists of components C103, C106, C107, C110, C111, C114, C115 and inductors L100, L101 and L102, which are a part of the SH100 assembly. The harmonic filter for lowband is pole zero design which gives greater attenuation in low frequencies where the harmonic energy of the transmitter is the greatest and less attenuation in high frequencies where there is less harmonic energy. The harmonic filter insertion loss is typically less than 0.8 dB.

## 2.4 Antenna Matching Network

The antenna matching network (T100) matches the antenna impedance with the harmonic filter to optimize the performance of the transmitter and receiver.

## 2.5 Power Control Integrated Circuit (PCIC)

The transmitter uses the PCIC (U102) to regulate the power output of the radio. To accomplish this, the voltage across R102 is sensed. This voltage drop is directly proportional to the current drawn in the final stage of the transmitter. This voltage is compared to a programmable reference inside the PCIC and the voltage on PCIC pin 4 adjusted. Pin 4 connects to the PA driver IC (U101) pin 1 via resistor R100 and varies RF output power of the driver. This controls the current drain of the final stage and sets the output power.

## 2.6 Temperature Cut Back Circuit

Temperature sensor VR101 and associated components are part of a temperature cut back circuit. This circuit senses the printed circuit board temperature around the transmitter circuits and outputs a DC voltage to the PCIC. If the DC voltage produced exceeds the set threshold of the PCIC, the transmitter output power decreases to reduce the transmitter temperature.

# 3.0 Lowband Receiver

(*Refer to Figure 2-2 and the Receiver Front End and Receiver Back End schematic diagrams)*

The Lowband receiver consists of a front end, back end, and automatic gain control circuits. Detailed descriptions of these stages are contained in the paragraphs that follow.

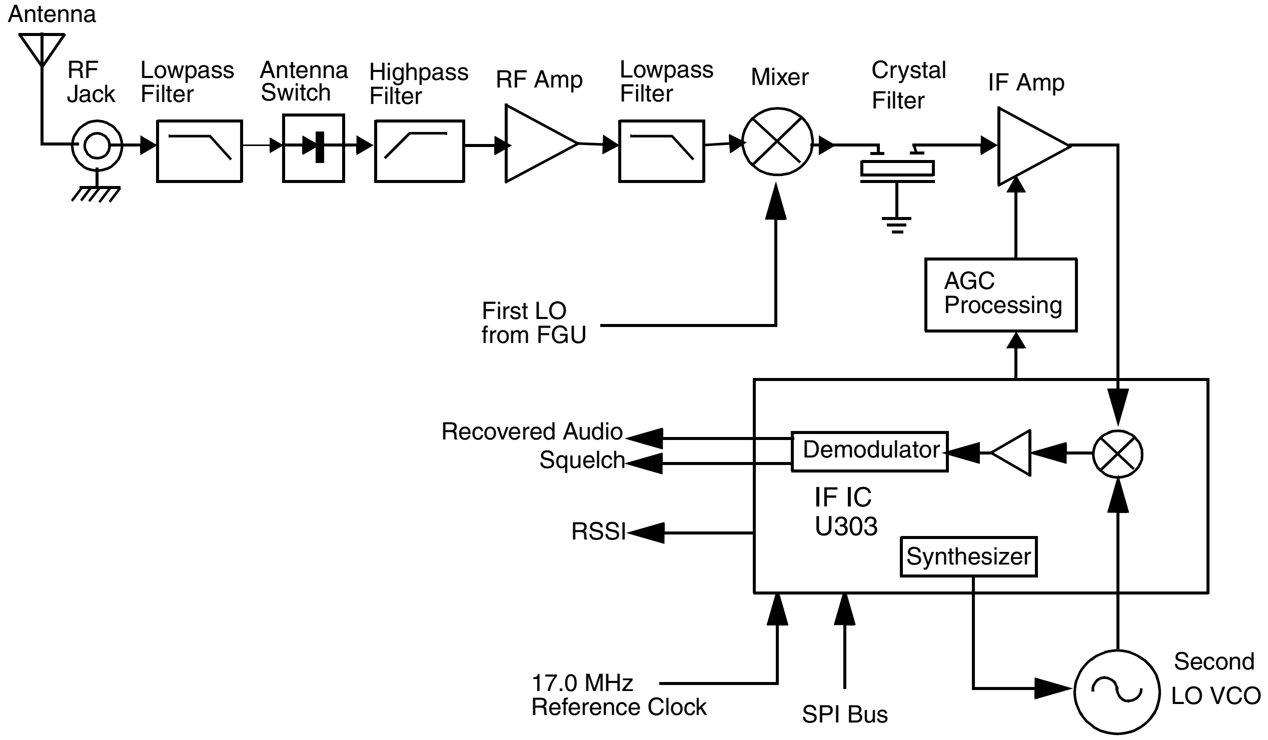



**Figure 2-2** Lowband Receiver Block Diagram.

## 3.1 Receiver Front-End

(*Refer to the Receiver Front End, Receiver Back end and Transmitter schematic diagrams*)

The RF signal received by the antenna is routed through the transmitter lowpass filter and antenna switch. These circuits are described in the transmitter section.The signal next passes through a highpass filter consisting of L501, L502, C538, C533 and C504. This filter serves to reject below band signals and has a 3 dB corner frequency of 27 MHz.

The output of the highpass filter is connected to an RF amp consisting of Q509 and associated biasing components. This is a BJT amplifier powered off 5 volts and has 13 dB of gain. The amplifier drives a lowpass filter consisting of L503, L504, L507, C534, C535, C536, C537 and C515. This filter is a pole zero design that filters off harmonic components from the RF amp. The 3 dB corner of this filter is at 56 MHz.

The output of the lowpass filter is connected to the passive double balanced mixer consisting of components T501, T502 and D501. After mixing with the first local oscillator up-converted to a 109.65 MHz IF signal.

The IF signal coming out of the mixer is transferred to the crystal filter (FL301) through a resistor pad (R507, R508 and R509) and a diplexer (C516 and L508). Matching to the input of the crystal filter is provided by L301, L302, C301 and C302. The 3 pole crystal filter provides the necessary selectivity and intermodulation protection.

## 3.2 Receiver Back-End

(*Refer to the Receiver Back End schematic diagram*)

The output of crystal filter FL301 is connected to the input of IF amplifier transistor U301. Components L303 and C348 and R301 form the termination for the crystal filter and the signal is coupled to one gate of U301 by C303. The IF amplifier is a dual gate MOSFET powered off of the 5 volt supply. The first gate receives the IF signal as indicated previously. The second gate receives a DC voltage from U302 which serves as an AGC control signal. This signal reduces the gain of the IF amplifier to prevent overload of the IF IC, U303. The gain can be varied from a maximum of 13 dB to an attenuation of 55 dB. The output IF signal from U301 is coupled into U303 (pin 3) via C306, R304 and L304 which provides matching for the IF amplifier and U303.

The IF signal applied to pin 3 of U303 is amplified, down-converted, filtered, and demodulated, to produce recovered audio at pin 27 of U303. This IF IC is electronically programmable, and the amount of filtering, which is dependent on the radio channel spacing, is controlled by the microprocessor. Additional filtering, once externally provided by the conventional ceramic filters, is replaced by internal filters in IF IC U303.

The IF IC uses a type of direct conversion process, whereby the externally generated second LO frequency is divided by two in U303 so that it is very close to the first IF frequency. The IF IC (U303) synthesizes the second LO and phase-locks the VCO to track the first IF frequency. The second LO is designed to oscillate at twice the first IF frequency because of the divide-by-two function in the IF IC.

In the absence of an IF signal, the VCO searches for a frequency, or its frequency will vary close to twice the IF frequency. When an IF signal is received, the VCO locks onto the IF signal. The second LO/VCO is a Colpitts oscillator built around transistor Q301. The VCO has a varactor diode, CR301, to adjust the VCO frequency. The control signal for the varactor is derived from a loop filter consisting of components C308, C309, and R310.

The IF IC (U303) also performs several other functions. It provides a received signal-strength indicator (RSSI) and a squelch output. The RSSI voltage is also used to control the automatic gain control (AGC) circuit at the back end.

The demodulated signal on pin 27 of U303 is also used for squelch control. The signal is routed to U404 (ASFIC) where squelch signal shaping and detection takes place. The demodulated audio signal is also routed to U404 for processing before going to the audio amplifier for amplification.

## 3.3 Automatic Gain Control (AGC)

(Refer to the Receiver Front End and Receiver Back End schematic diagrams)

The automatic gain control circuit provides automatic reduction of gain to prevent overloading of backend circuits. This is achieved by lowering the voltage on one gate of U301 which will reduce the drain current in that part and lower its gain.

The Radio Signal Strength Indicator (RSS I) voltage signal for the IF IC (U303) is used to drive the AGC processing circuitry consisting of R306, R307, R308, R309, C307 and U302. As the received signal gets stronger, the RSSI line will rise. When the RSSI line passes a certain threshold, the voltage at the output of U302 will begin to drop. This voltage is connected to one gate of IF amplifier U301 through resistor R305. As this voltage decreases, it will lower the drain current in U301 and reduce the gain of the stage. This will limit the power incident on the IF IC, U303.

# 4.0 Frequency Generation Circuit

(*Refer to Figure 2-3, the Synthesizer and Voltage controlled Oscillator schematic diagrams*)

The frequency generation circuit is composed of Low Voltage Fractional-N synthesizer U205 and discrete RX VCO, TX VCO and buffers as well other supporting circuitry. The synthesizer block diagram illustrates the interconnect and support circuitry used in the region. Refer to the schematic for the reference designators.

The synthesizer is powered by regulated 5V and 3.3V. The 5 volt signal to the synthesizer as well as the rest of the radio is provided by U204. The 3.3 v signal is provided from U200 in the controller. The 5V signal goes to pins 13 and 30 while the 3.3V signal goes to pins 5, 20, 34 and 36 of U201. The synthesizer in turn generates a superfiltered 4.3V which powers the VCOs and buffers.

In addition to the VCO, the synthesizer also interfaces with the logic and ASFIC circuitry. Programming for the synthesizer is accomplished through the data, clock and chip select lines (pins 7, 8 and 9) from the microprocessor, U409. A 3.3V dc signal from pin 4 indicates to the microprocessor that the synthesizer is locked.

Transmit modulation from the ASFIC is supplied to pin 10 of U205. Internally the audio is digitized by the Fractional-N and applied to the loop divider to provide the low-port modulation. The audio runs through an internal attenuator for modulation balancing purposes before going out at pin 41 to the VCO.

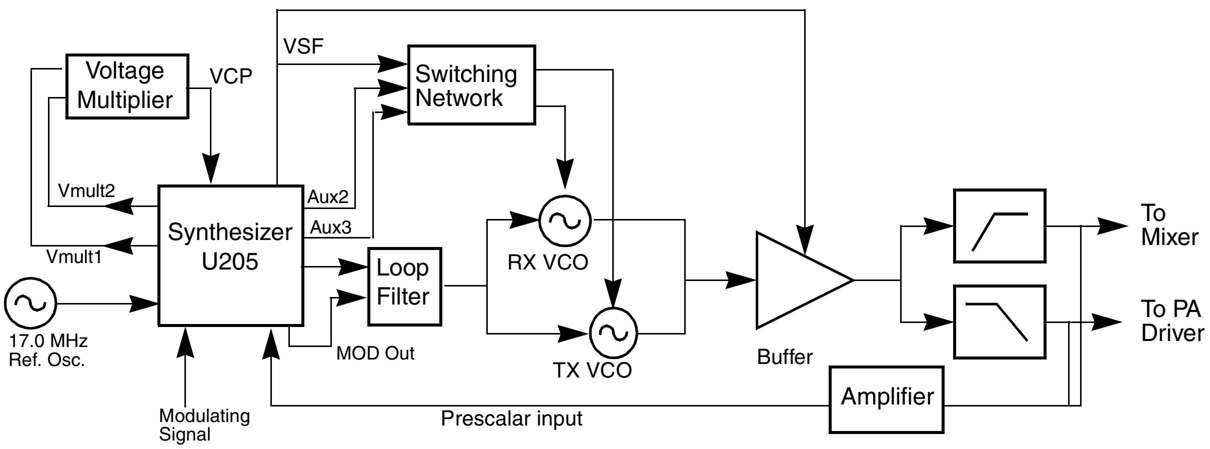



**Figure 2-3** Lowband Frequency Generation Unit Block Diagram

## 4.1 Synthesizer

(Refer to Figure 2-4 and the Synthesizer schematic diagram)

The Fractional-N synthesizer, shown in Figure 2-4, uses a 17.0 MHz crystal (Y201) to provide a reference for the system. Along with being used in the LVFracN, the 17.0 MHz signal is provided at pin 19 of U205 for use by the ASFIC and LVZIF.

The LVFractN IC (U205) further divides this by 8 internally to give 2.125 MHz to be used as the reference frequency in the frequency synthesis. While UHF and VHF can use other references, (divide by 7 or divide by 7/8), only the divide by 8 function is valid for lowband.

The internal oscillator device in the LVFracN together with C236, C237, C242, R219, CR211 and Y201 comprise the reference oscillator. This oscillator is temperature compensated is capable of 2.5 ppm stability over temperatures of -30 to 85°C. There is temperature compensation information that is unique to each crystal contained on Y201 that is programmed into the radio when built.

The loop filter consists of components C256, C257, C259, R224, R225 and R228. This circuit provides the necessary dc steering voltage for the VCO and determines the amount of noise and spur passing through.

To achieve fast locking for the synthesizer, an internal adapt charge pump provides higher current at pin 45 of U205 to put the synthesizer within lock range. The required frequency is then locked by normal mode charge pump at pin 43.

Both the normal and adapt charge pumps get their supply from the inductive voltage multiplier made up of C247, C249, C283-C286, D210, D211, R285 and R286.
This circuit provides 13.3V at U205, pin 47.

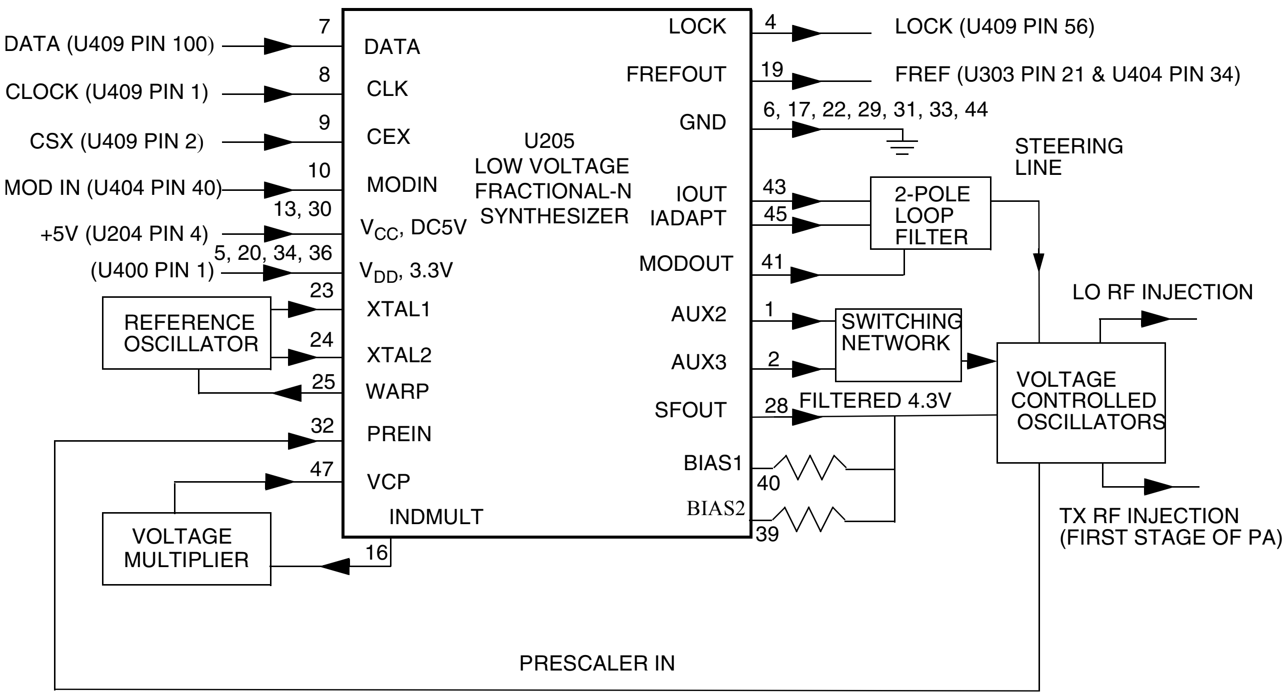



**Figure 2-4** Lowband Synthesizer Block Diagram.

## 4.2 Voltage Controlled Oscillator (VCO)

(*Refer to the Voltage Controlled Oscillator schematic diagram*)

### 4.2.1 Receive VCO

The receive VCO is a Colpitts type design and using two active devices in parallel, Q202 and Q204. The oscillator is powered off of the 4.3 volt super filter supply when the AUX3 line goes low. The oscillator operates from 139 to 152 MHz for range 1 and 145 to 160 MHz for range 2. The frequency is tuned by varactor diodes CR201 and CR202.

### 4.2.2 Transmit VCO

The transmit VCO is a Hartley type design with active devices Q203. The oscillator is powered off of the 4.3 volt super filter supply when the AUX2 line goes low. The oscillator operates from 29.7 to 42 MHz for Range 1 and 35 to 50 MHz for Range 2. The frequency is tuned by varactor diodes in U203. Note that the values of the inductive tap, L208 and L209, and the capacitor C215 which couples the varactor to the oscillator tank vary between the ranges.

### 4.2.3 Buffer

Both the receive and transmit VCO are fed to a buffer amplifier Q201. This is a BJT amplifier that boosts the signal levels to +4 dBm and provides reverse isolation to the oscillators. The amplifier is powered off the 4.3 volt super filter supply and the feed network is combined with the transmit filter.

### 4.2.4 Diplexer and Output Filters

The output of the buffer drives a pair of parallel filters. One filter is a lowpass filter in the TX path that passes 29.7 - 50 MHz signals for the transmitter into the power amplifier while rejecting the receive LO injection signals at 139 - 160 MHz. This filter is comprised of L204, L211, L212, C230 and C231.

The other filter is a highpass filter which passes 139 - 160 MHz signals for the receive LO into the mixer while rejecting the transmit injection signals at 29.7 -50 MHz. This filter is comprised of C228,C229,C235 and L215.

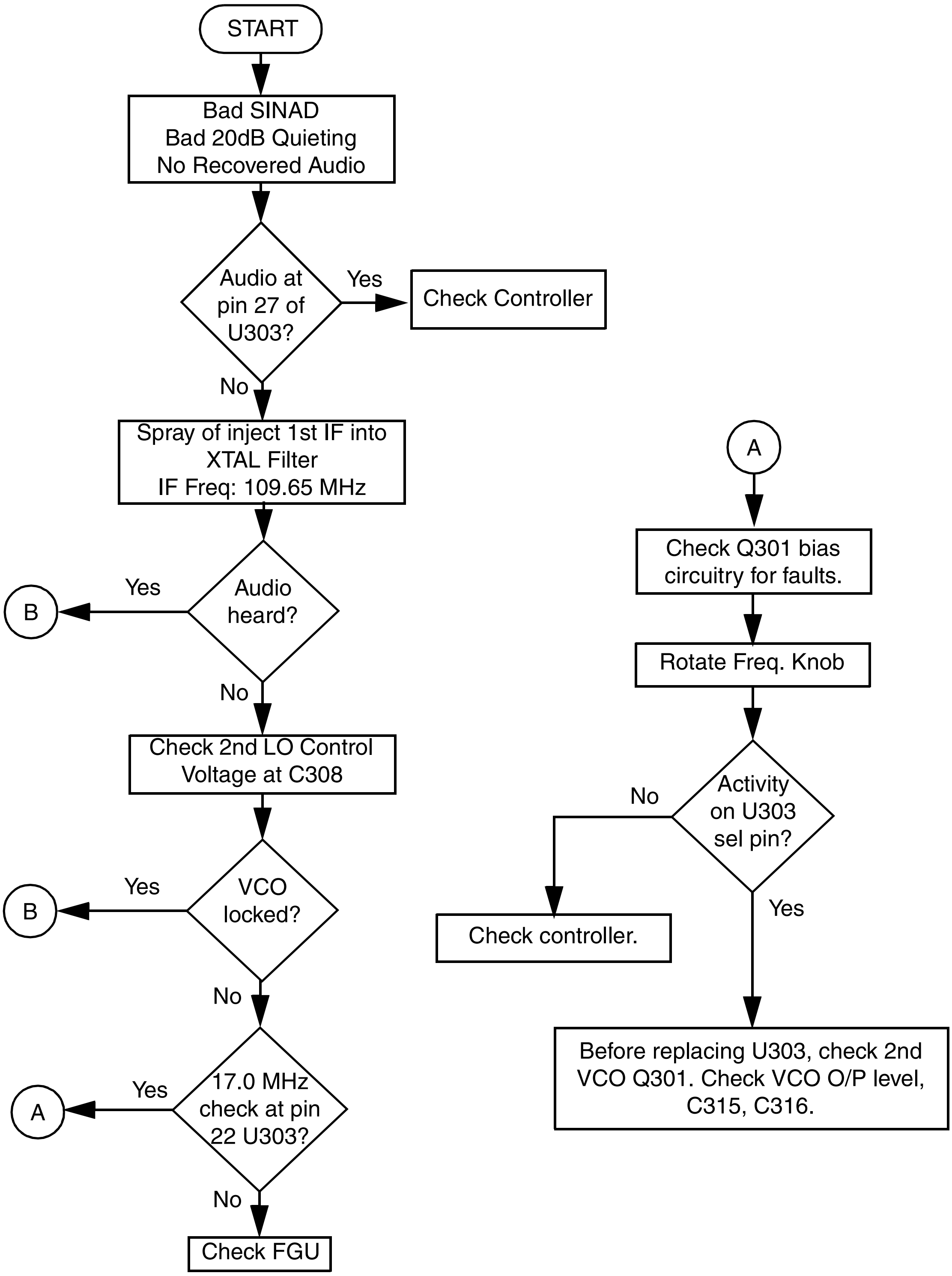
### 4.2.5 Prescaler Feedback

The prescaler input signal for receive and transmit is tapped off the outputs of each filter by resistors R234 and R238. This signal is routed to the buffer amplifier consisting of components C287, Q288, R287, R288 and R289. The output of this buffer feeds U205 pin 32. After frequency comparison in the synthesizer, current is transferred in the loop filter and a control voltage is generated at the output of the loop filter to adjust the frequency of the VCO. This voltage is a DC voltage between 3.5V and 9.5V when the PLL is locked on frequency.

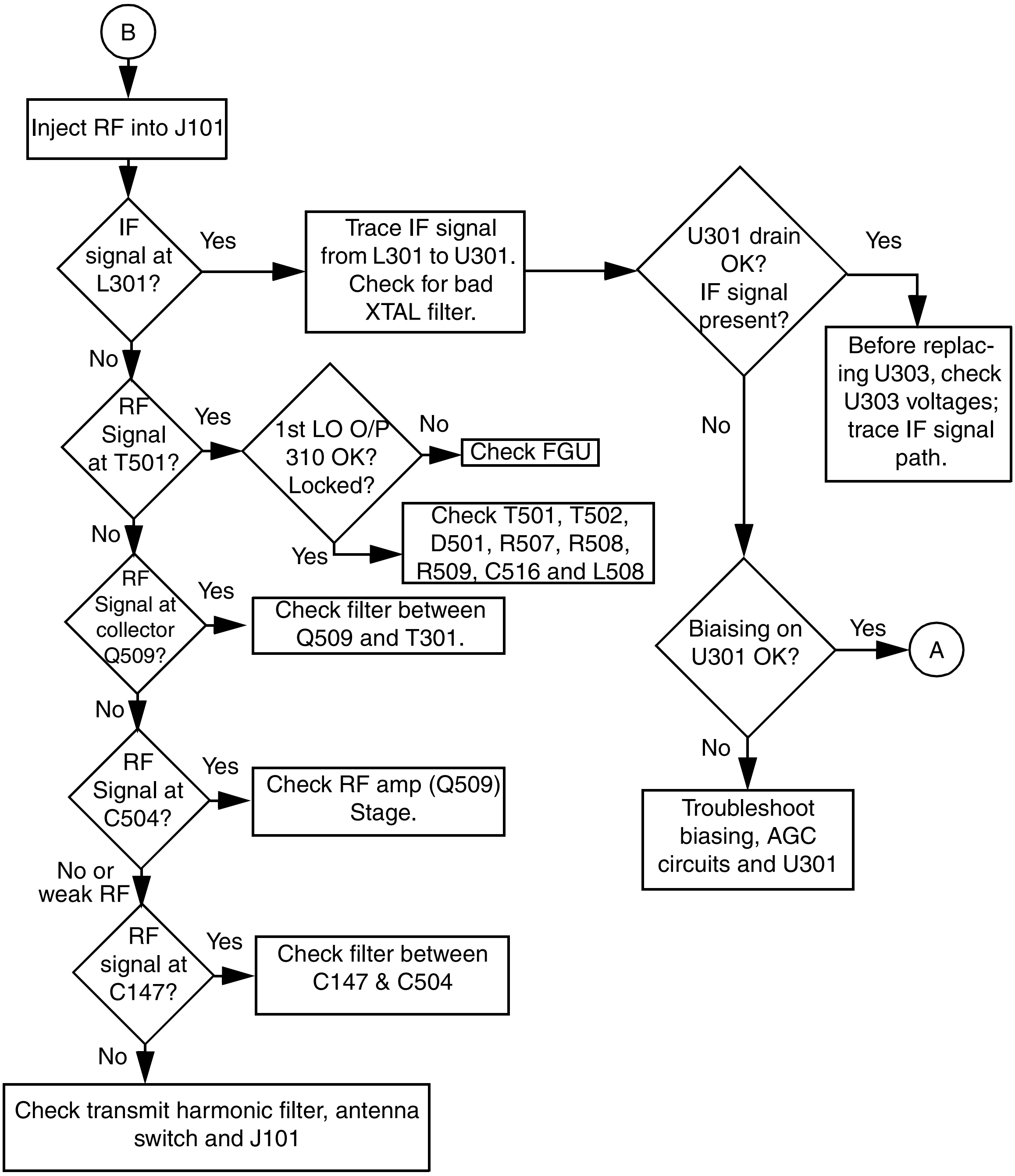
# Chapter 3

# TROUBLESHOOTING CHARTS

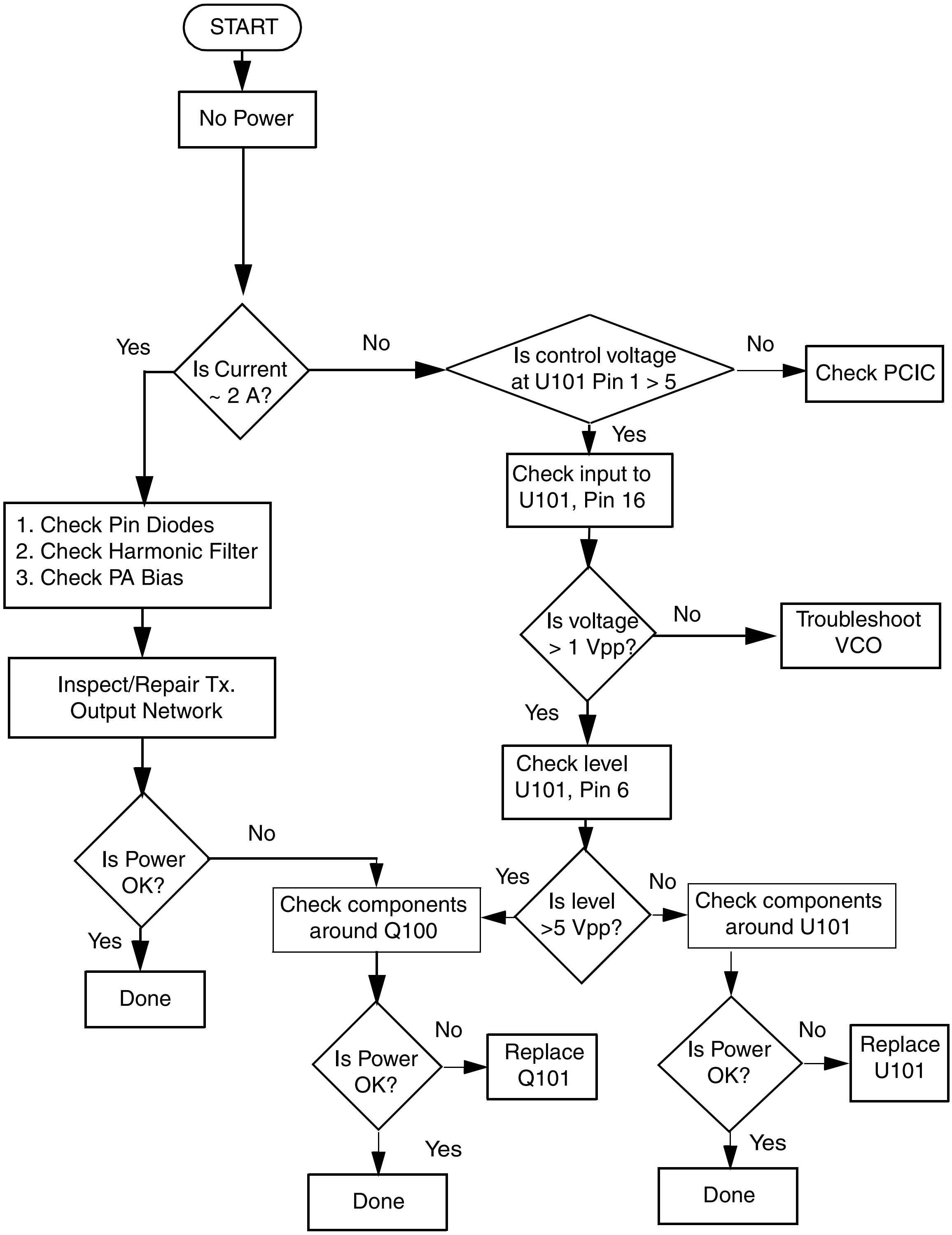
## 1.0 Receiver (Sheet 1 of 2)



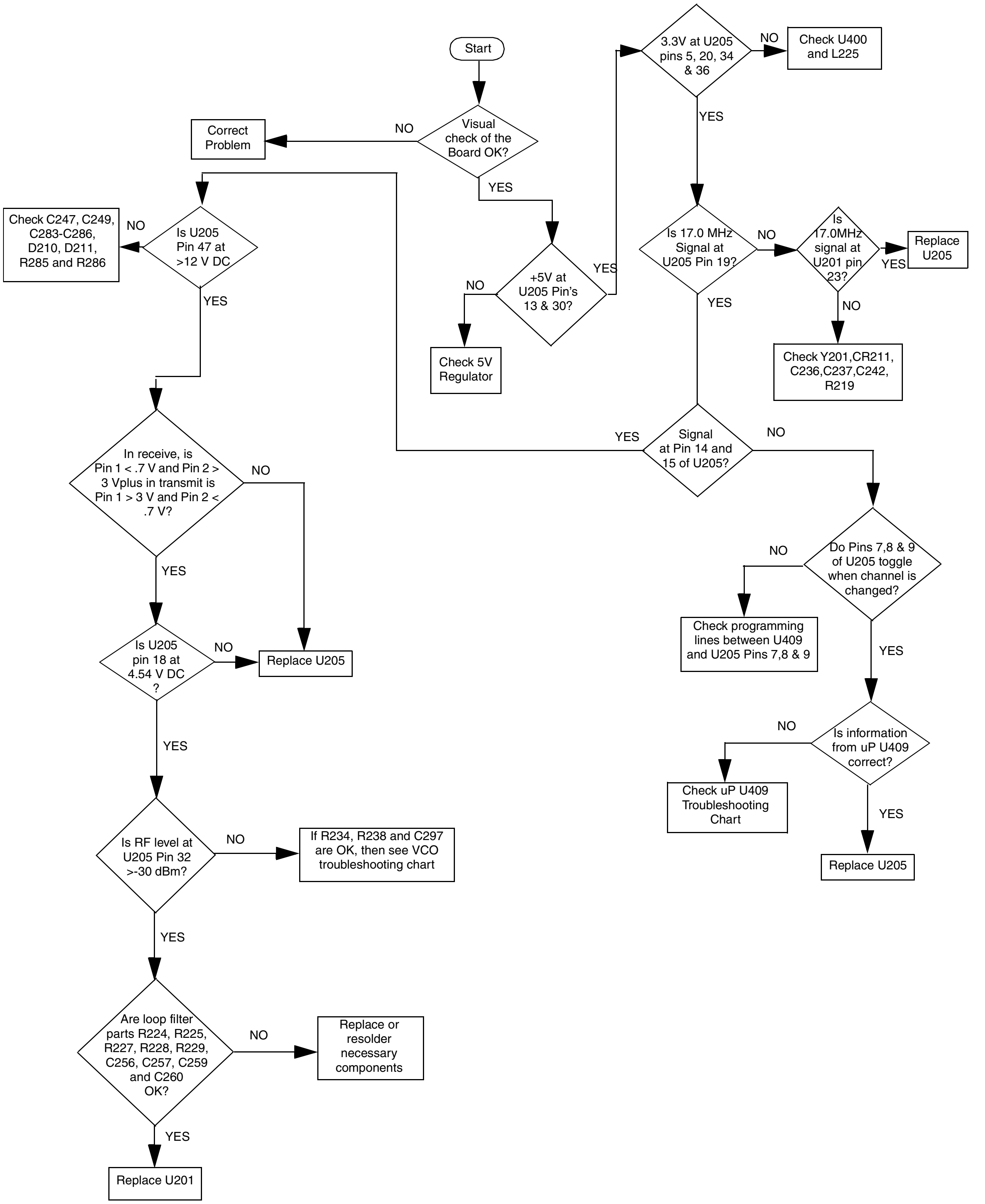
## 2.0 Receiver (Sheet 2 of 2)



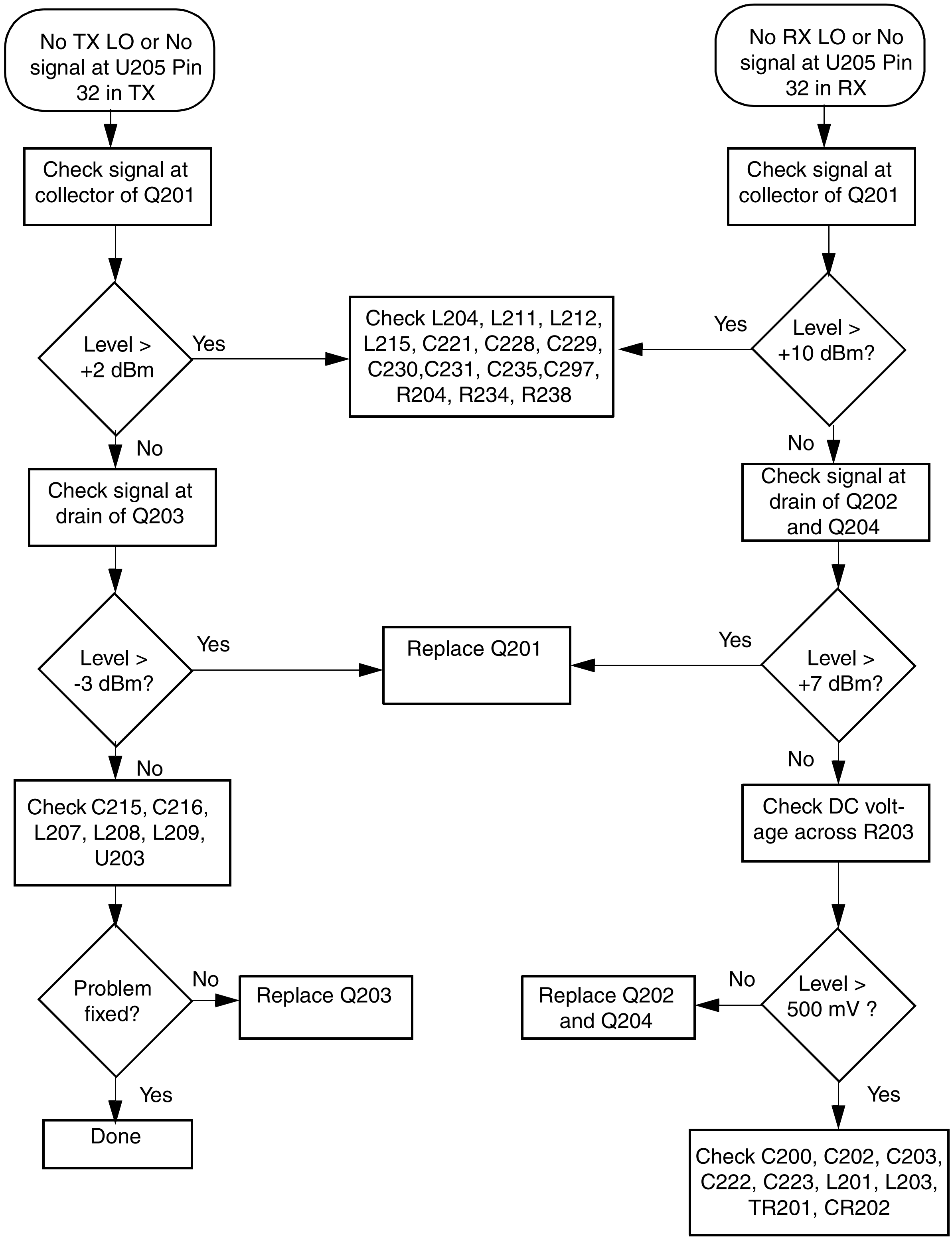
# 3.0 Transmitter



# 4.0 Synthesizer



## 5.0 Voltage Controlled Oscillator



# Chapter 4

# LOWBAND PCB/SCHEMATICS/PARTS LIST

## 1.0 Allocation of Schematics and Circuit Boards

### 1.1 Controller Circuits

The Lowband circuits are contained on the printed circuit board (PCB) which also contains the Controller circuits. This chapter shows the schematics for the Lowband circuits only, refer to the Controller section for details of the related Controller circuits. The PCB component layouts and the Parts Lists in this chapter show both the Controller and Lowband circuit components. The Lowband schematics and the related PCB and parts list are shown in the Table below.

**Table 4-1** Lowband Diagrams and Parts